# NCR125W-125M

## SCR

Rev.01 - 24 September 2019 Product data sheet

## 1. General description

Planar passivated SCR with sensitive gate in a SOT223 surface mountable plastic package. This SCR is designed to be interfaced directly to microcontrollers, logic integrated circuits and other low power gate trigger circuits.

## 2. Features and benefits

- Sensitive gate
- High surge current capability
- High voltage capability
- Planar passivated for voltage ruggedness and reliability
- Direct triggering from low power drivers and logic ICs
- Surface mountable package

## 3. Applications

- Ground Fault Circuit Interrupter (GFCI)
- GFCI Socket
- Residual Current Circuit Breaker with Overcurrent Protection (RCBO)
- Arc Fault Circuit Interrupter (AFCI)

## 4. Quick reference data

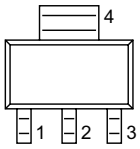
**Table 1. Quick reference data**

| Symbol | Parameter | Conditions | Values | Unit |
|---|---|---|---|---|
| $V_{DRM}$ | repetitive peak off-state voltage | | 1250 | V |
| $I_{T(RMS)}$ | RMS on-state current | half sine wave; $T_c \leq 111$ °C; Fig. 1; Fig. 2; Fig. 3 | 1.25 | A |
| $I_{TSM}$ | non-repetitive peak on-state current | half sine wave; $T_{j(init)} = 25$ °C; $t_p = 10$ ms; Fig 4; Fig 5 | 20 | A |
| | | half sine wave; $T_{j(init)} = 25$ °C; $t_p = 8.3$ ms | 22 | A |
| $T_j$ | junction temperature | | 125 | °C |

| Symbol | Parameter | Conditions | | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|---|
| **Static characteristics** | | | | | | | |
| $I_{GT}$ | gate trigger current | $V_D$ = 12 V; $R_L$ = 140 Ω; $T_j$ = 25 °C; Fig. 8 | | 1 | - | 100 | µA |
| $I_H$ | holding current | $V_D$ = 12 V; $R_{GK}$ = 220 Ω; $T_j$ = 25 °C; Fig. 10 | | - | - | 10 | mA |
| $V_T$ | on-state voltage | $I_T$ = 2.5 A; $T_j$ = 25 °C; Fig. 11 | | - | - | 1.5 | V |
| **Dynamic characteristics** | | | | | | | |
| $dV_D/dt$ | rate of rise of off-state voltage | $V_{DM}$ = 838 V; $T_j$ = 125 °C; $R_{GK}$ = 220 Ω; ($V_{DM}$ = 67% of $V_{DRM}$); exponential waveform | | 200 | - | - | V/µs |

## 5. Pinning information

**Table 2. Pinning information**

| Pin | Symbol | Description | Simplified outline | Graphic symbol |
|---|---|---|---|---|
| 1 | K | cathode |  |  |
| 2 | A | anode | | |
| 3 | G | gate | | |
| 4 | A | mounting base; connected to anode | | |





## 6. Ordering information

**Table 3. Ordering information**

| Type number | Package Name | Orderable part number | Packing method | Small packing quantity | Package version | Package issue date |
|---|---|---|---|---|---|---|
| NCR125W-125M | SOT223 | NCR125W-125MX | Reel | 1000 | SOT223 | 16-Mar-2006 |

## 7. Marking

**Table 4. Marking codes**

| Type number | Marking codes |
|---|---|
| NCR125W-125M | 125-125M |

# 8. Limiting values

**Table 5. Limiting values**

*In accordance with the Absolute Maximum Rating System (IEC 60134).*

| Symbol | Parameter | Conditions | Values | Unit |
|---|---|---|---|---|
| $V_{DRM}$ | repetitive peak off-state voltage | | 1250 | V |
| $V_{RRM}$ | repetitive peak reverse voltage | | 1250 | V |
| $I_{T(AV)}$ | average on-state current | half sine wave; $T_c \leq 111$ °C; | 0.8 | A |
| $I_{T(RMS)}$ | RMS on-state current | half sine wave; $T_c \leq 111$ °C; Fig. 1; Fig. 2; Fig. 3 | 1.25 | A |
| $I_{TSM}$ | non-repetitive peak on-state current | half sine wave; $T_{j(init)} = 25$ °C; $t_p = 10$ ms; Fig 4; Fig 5 | 20 | A |
| | | half sine wave; $T_{j(init)} = 25$ °C; $t_p = 8.3$ ms | 22 | A |
| $I^2t$ | $I^2t$ for fusing | $t_p = 10$ ms; sine-wave pulse | 2 | $A^2s$ |
| $dI_T/dt$ | rate of rise of on-state current | $I_G = 0.1$ mA; f = 50 Hz; $T_j = 125$ °C | 100 | A/µs |
| | non-repetitive critical current rate of rise at break over, refer Fig. 14 | | 200 | A/µs |
| $I_{GM}$ | peak gate current | $t_p = 20$ us; $T_j = 125$ °C | 1.2 | A |
| $P_{GM}$ | peak gate power | | 5 | W |
| $P_{G(AV)}$ | average gate power | over any 20 ms period | 0.2 | W |
| $T_{stg}$ | storage temperature | | -40 to 150 | °C |
| $T_j$ | junction temperature | | -40 to 125 | °C |

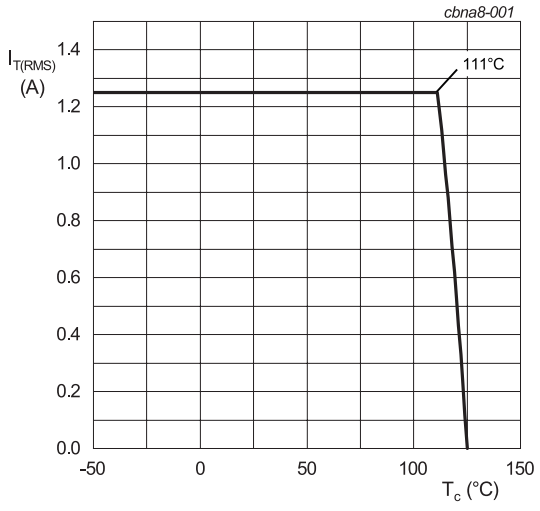
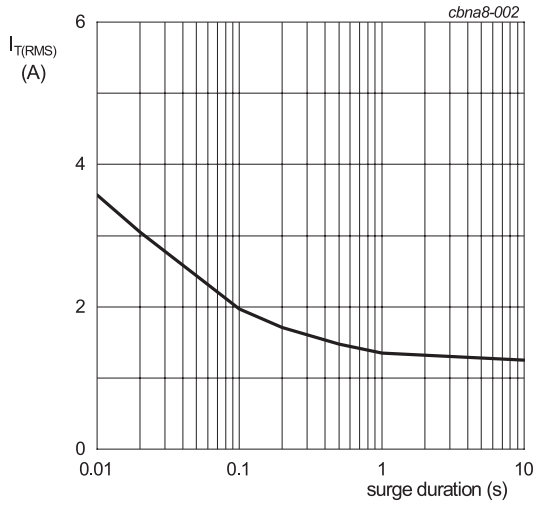
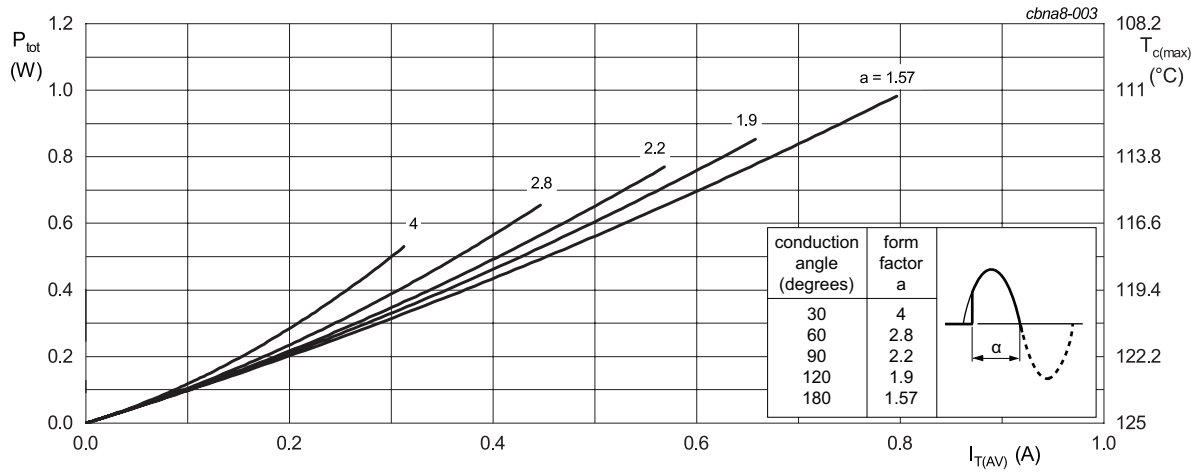



**Fig. 1. RMS on-state current as a function of case temperature; maximum values**




f = 50 Hz; $T_c = 111$ °C

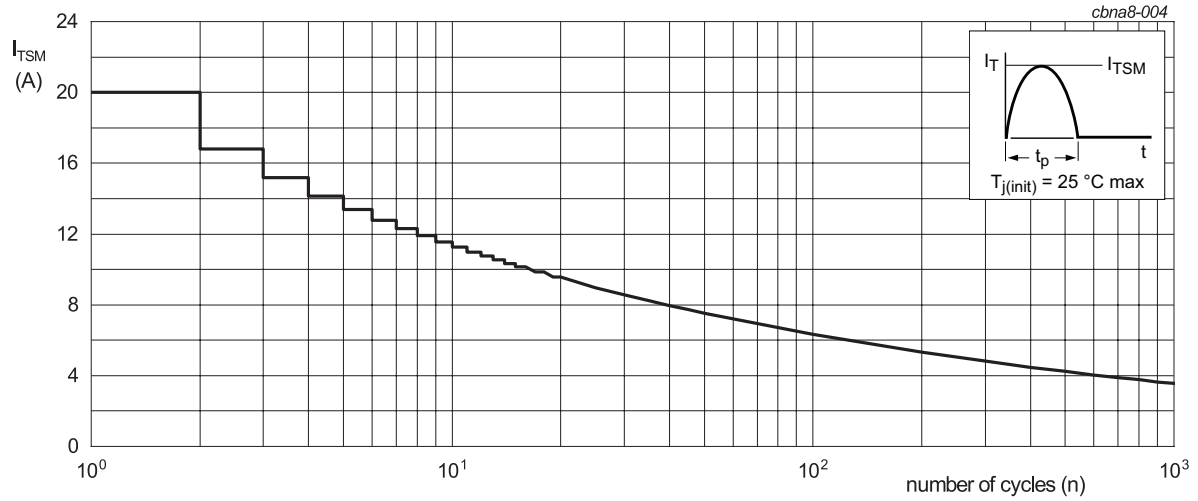
**Fig. 2. RMS on-state current as a function of surge duration; maximum values**




α = conduction angle

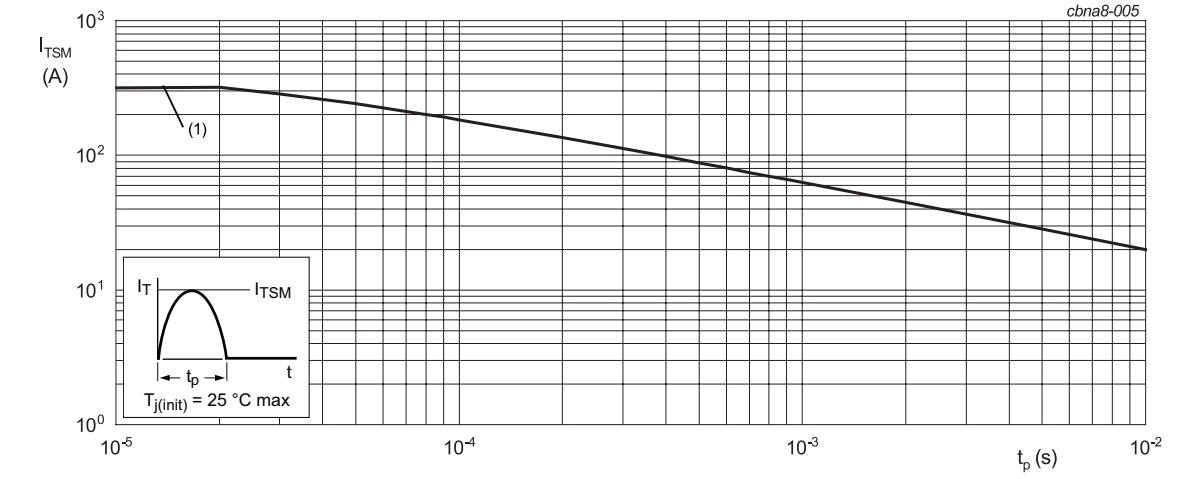
a = form factor = $I_{T(RMS)}$ / $I_{T(AV)}$

**Fig. 3. Total power dissipation as a function of RMS on-state current; maximum values**




f = 50 Hz

**Fig. 4. Non-repetitive peak on-state current as a function of the number of sinusoidal current cycles; maximum values**




$t_p \leq 10$ ms

(1) $dI_T/dt$ limit

**Fig. 5. Non-repetitive peak on-state current as a function of pulse duration; maximum values**

# 9. Thermal characteristics

**Table 6. Thermal characteristics**

| Symbol | Parameter | Conditions | | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|---|
| $R_{th(j-c)}$ | thermal resistance from junction to case | Fig 6 | | - | - | 14 | K/W |
| $R_{th(j-a)}$ | thermal resistance from junction to ambient | in free air; printed circuit board mounted: minimum footprint; Fig 7 | | - | 130 | - | K/W |

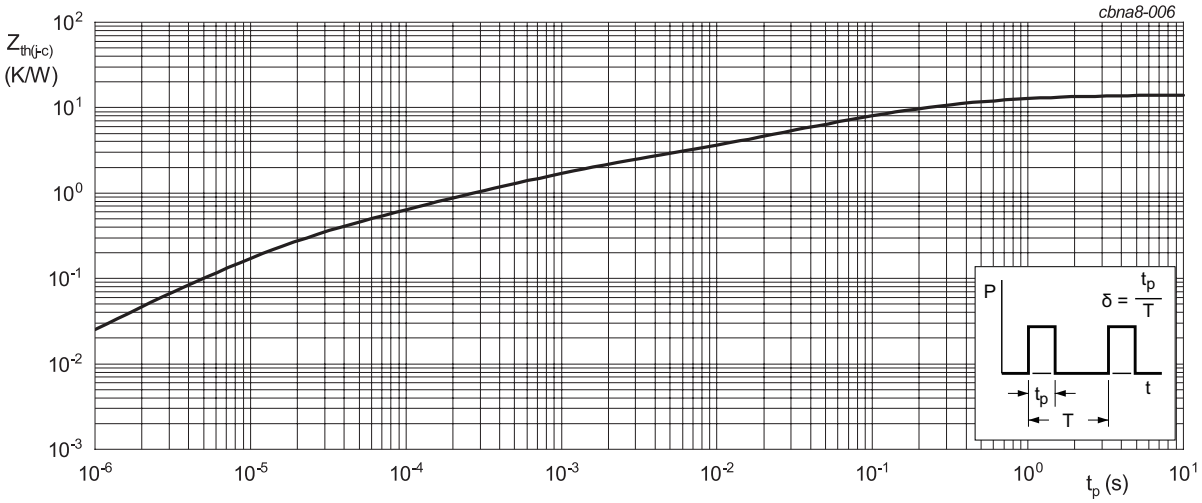
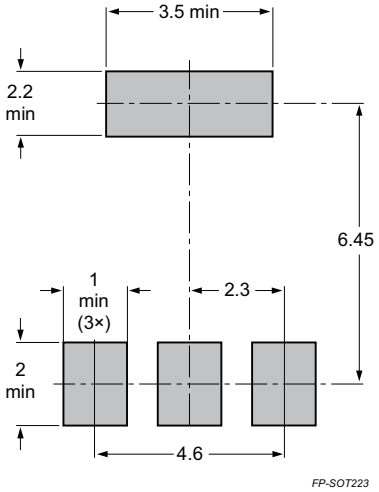



**Fig. 6. Transient thermal impedance from junction to case as a function of pulse duration**




All dimensions are in mm

**Fig. 7. Minimum footprint SOT223**

# 10. Characteristics

**Table 7. Characteristics**

| Symbol | Parameter | Conditions | | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|---|
| **Static characteristics** | | | | | | | |
| $I_{GT}$ | gate trigger current | $V_D$ = 12 V; $R_L$ = 140 Ω; $T_j$ = 25 °C; Fig. 8 | | 1 | - | 100 | µA |
| $V_{GT}$ | gate trigger voltage | $V_D$ = 12 V; $R_L$ = 140 Ω; $T_j$ = 25 °C; Fig. 12 | | - | 0.6 | 0.8 | V |
| $V_{GD}$ | gate non-trigger voltage | $V_D$ = $V_{DRM}$; $R_L$ = 33 kΩ; $R_{GK}$ = 220 Ω; $T_j$ = 125 °C | | 0.1 | - | - | V |
| $V_{RG}$ | gate reverse voltage | $I_{RG}$ = 2 mA; $T_j$ = 25 °C | | 10 | - | - | V |
| $I_L$ | latching current | $I_T$ = 0.1 A; $R_{GK}$ = 220 Ω; $T_j$ = 25 °C; Fig. 9 | | - | - | 12 | mA |
| $I_H$ | holding current | $V_D$ = 12 V; $R_{GK}$ = 220 Ω; $T_j$ = 25 °C; Fig. 10 | | - | - | 10 | mA |
| $V_T$ | on-state voltage | $I_T$ = 2.5 A; $T_j$ = 25 °C; Fig. 11 | | - | - | 1.5 | V |
| $I_D$ | off-state current | $V_D$ = 1250 V; $R_{GK}$ = 220 Ω; $T_j$ = 25 °C | | - | - | 1 | µA |
| | | $V_D$ = 1250 V; $R_{GK}$ = 220 Ω; $T_j$ = 125 °C | | - | - | 100 | µA |
| $I_R$ | reverse current | $V_D$ = 1250 V; $R_{GK}$ = 220 Ω; $T_j$ = 25 °C | | - | - | 1 | µA |
| | | $V_D$ = 1250 V; $R_{GK}$ = 220 Ω; $T_j$ = 125 °C | | - | - | 100 | µA |
| **Dynamic characteristics** | | | | | | | |
| $dV_D/dt$ | rate of rise of off-state voltage | $V_{DM}$ = 838 V; $T_j$ = 125 °C; $R_{GK}$ = 220 Ω; ($V_{DM}$ = 67% of $V_{DRM}$); exponential waveform | | 200 | - | - | V/µs |
| $V_O$ | threshold voltage | $T_j$ = 125 °C | | - | - | 0.936 | V |
| $R_S$ | dynamic resistance | $T_j$ = 125 °C | | - | - | 152 | mΩ |

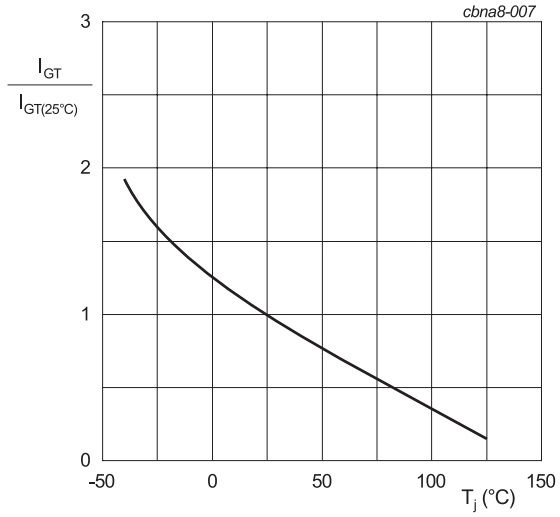



**Fig. 8. Normalized gate trigger current as a function of junction temperature**

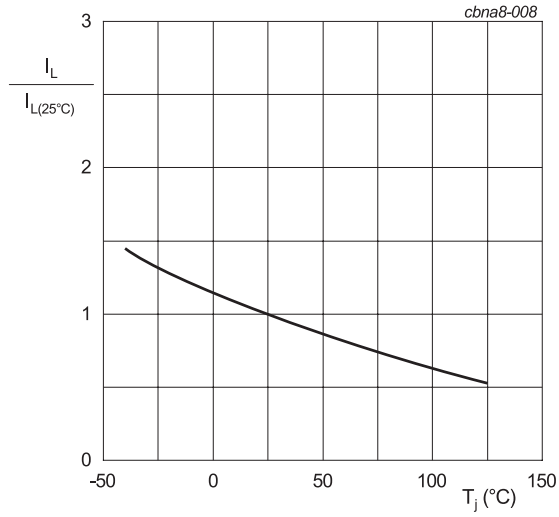



**Fig. 9. Normalized latching current as a function of junction temperature**

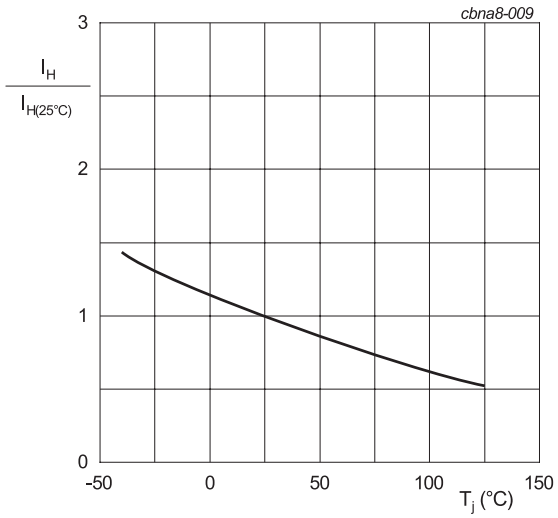
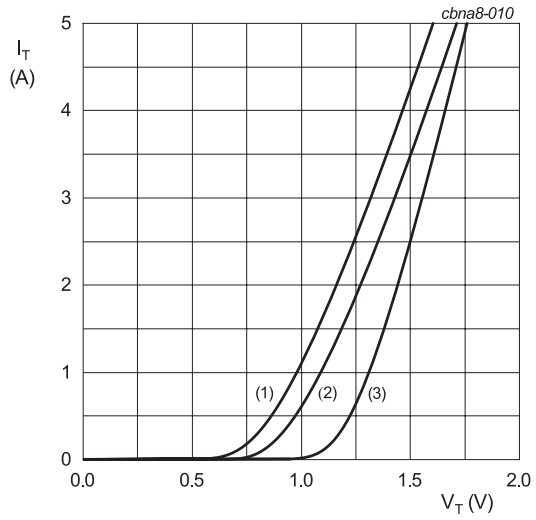



**Fig. 10. Normalized holding current as a function of junction temperature**




$V_o$ = 0.936 V; $R_s$ = 0.1520 Ω
(1) $T_j$ = 150 °C; typical values
(2) $T_j$ = 150 °C; maximum values
(3) $T_j$ = 25 °C; maximum values

**Fig. 11. On-state current as a function of on-state voltage**

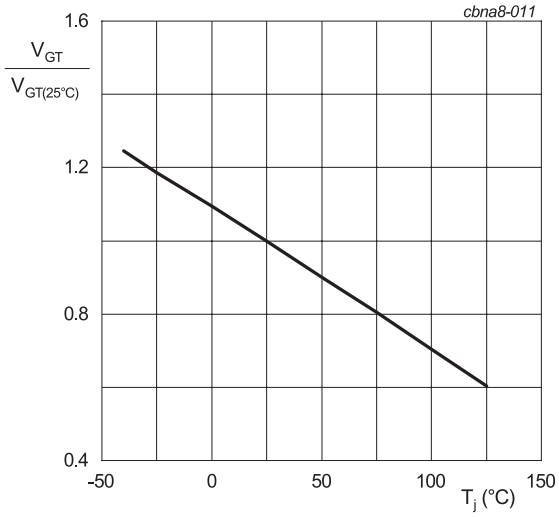



**Fig. 12. Normalized gate trigger voltage as a function of junction temperature**

## 11. AC line transient voltage ruggedness

NCR125W-125M has over voltage self-protected function, it can safely withstand AC line direct surge voltages by switching to on-state (for less than 10 ms on 50 Hz mains) to dissipate energy shocks through the load. The load limits the current through NCR125W-125M. The self-protection against over-voltage is based on an overvoltage crowbar technology. This safety feature works even with high turn-on current ramp up.

The NCR125W-125M recovers its blocking voltage capability after the direct surge and the next zero current crossing. Typical current and voltage as below according to the IEC 61000-4-5 standard conditions. Such a non-repetitive test can be done at least 10 times.

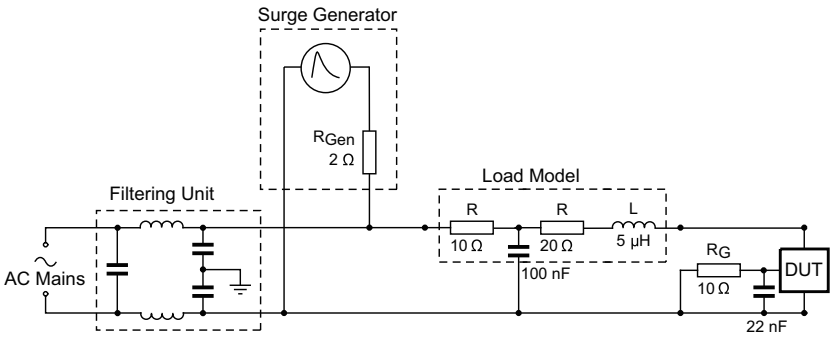



**Fig. 13. Overvoltage ruggedness test circuit for IEC 61000-4-5 standards**

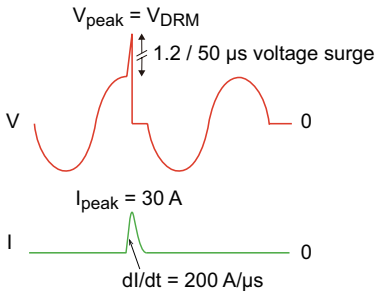
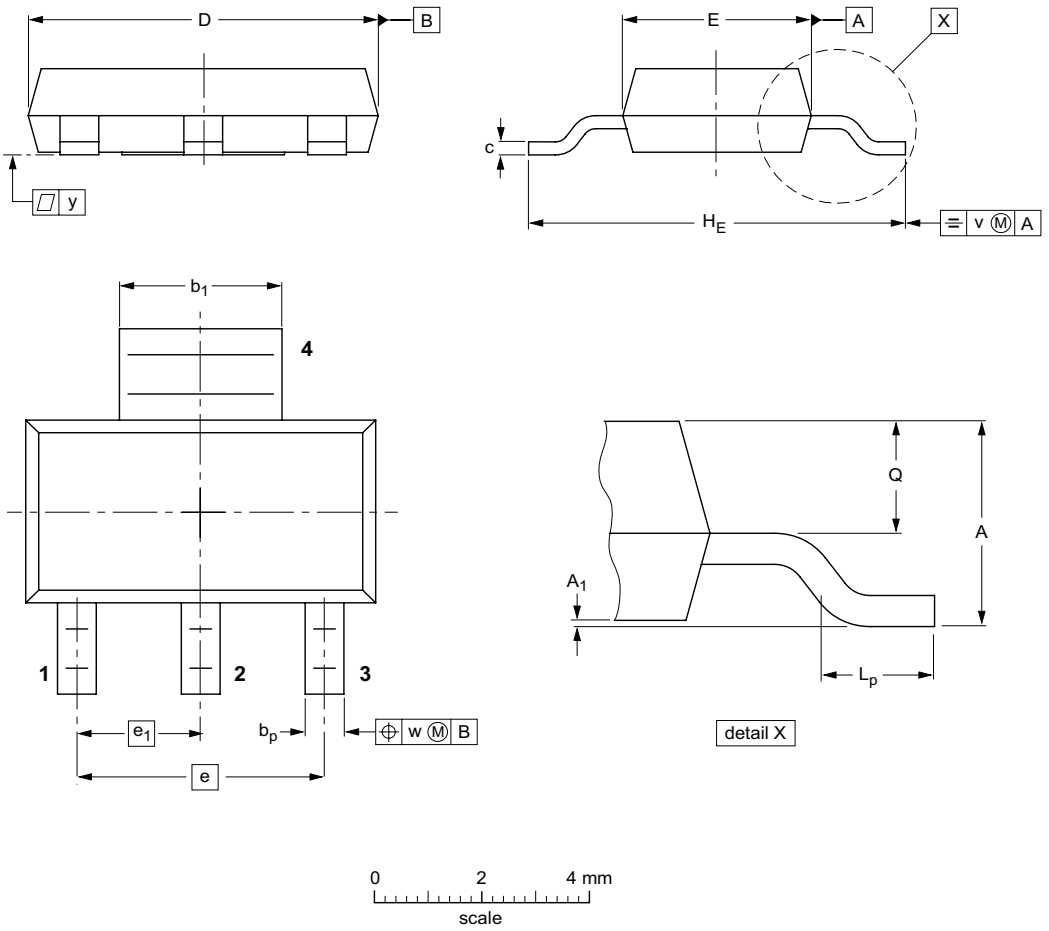



**Fig. 14. Typical current and voltage waveforms across NCR125W-125M during IEC 61000-4-5 standard test**

## 12. Package outline

**Plastic surface-mounted package with increased heatsink; 4 leads** **SOT223**




**DIMENSIONS (mm are the original dimensions)**

| UNIT | A | $A_1$ | $b_p$ | $b_1$ | c | D | E | e | $e_1$ | $H_E$ | $L_p$ | Q | v | w | y |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| mm | 1.8<br>1.5 | 0.10<br>0.01 | 0.80<br>0.60 | 3.1<br>2.9 | 0.32<br>0.22 | 6.7<br>6.3 | 3.7<br>3.3 | 4.6 | 2.3 | 7.3<br>6.7 | 1.1<br>0.7 | 0.95<br>0.85 | 0.2 | 0.1 | 0.1 |

| OUTLINE VERSION | REFERENCES | | | | EUROPEAN PROJECTION | ISSUE DATE |
|---|---|---|---|---|---|---|
| | IEC | JEDEC | JEITA | | | |
| SOT223 | | | SC-73 | | | ~~04-11-10~~<br>06-03-16 |

**Fig. 15. Package outline SOT223**

# 13. Legal information

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| Document status [1][2] | Product status [3] | Definition |
|---|---|---|
| Objective [short] data sheet | Development | This document contains data from the objective specification for product development. |
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**Date of release: 24 September 2019**