

1. General description

Planar passivated sensitive gate four quadrant triac in a TO220F plastic package intended for use in general purpose bidirectional switching and phase control applications. This sensitive gate "series E" triac is intended to be interfaced directly to microcontrollers, logic integrated circuits and other low power gate trigger circuits.

2. Features and benefits

- High blocking voltage capability
- Planar passivated for voltage ruggedness and reliability
- Sensitive gate
- Triggering in all four quadrants
- Isolated package
- Direct triggering from low power drivers and logic ICs
- Low holding current for small load currents and lowest EMI at commutation

3. Applications

- General purpose motor control
- General purpose switching

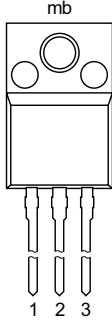

4. Quick reference data

Table 1. Quick reference data

Symbol	Parameter	Conditions	Values			Unit
Absolute maximum rating						
V_{DRM}	repetitive peak off-state voltage		600			V
$I_{T(RMS)}$	RMS on-state current	full sine wave; $T_h \leq 92\text{ °C}$; Fig. 1 ; Fig. 2 ; Fig. 3	4			A
I_{TSM}	non-repetitive peak on-state current	full sine wave; $T_{j(initial)} = 25\text{ °C}$; $t_p = 20\text{ ms}$; Fig. 4 ; Fig. 5	25			A
Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Static characteristics						
I_{GT}	gate trigger current	$V_D = 12\text{ V}$; $I_T = 0.1\text{ A}$; T2+ G+; $T_j = 25\text{ °C}$; Fig. 7	-	2.5	10	mA
		$V_D = 12\text{ V}$; $I_T = 0.1\text{ A}$; T2+ G-; $T_j = 25\text{ °C}$; Fig. 7	-	4	10	mA
		$V_D = 12\text{ V}$; $I_T = 0.1\text{ A}$; T2- G-; $T_j = 25\text{ °C}$; Fig. 7	-	5	10	mA
		$V_D = 12\text{ V}$; $I_T = 0.1\text{ A}$; T2- G+; $T_j = 25\text{ °C}$; Fig. 7	-	11	25	mA
I_H	holding current	$V_D = 12\text{ V}$; $T_j = 25\text{ °C}$; Fig. 9	-	2.2	15	mA

5. Pinning information

Table 2. Pinning information

Pin	Symbol	Description	Simplified outline	Graphic symbol
1	T1	main terminal 1		 sym051
2	T2	main terminal 2		
3	G	gate		
mb	n.c.	mounting base; isolated		

6. Ordering information

Table 3. Ordering information

Type number	Package Name	Orderable part number	Packing method	Small packing quantity	Package version	Package issue date
BT136X-600E	TO220F	BT136X-600E,127	Tube	50	SOT186A	14-Nov-2013
BT136X-600E/DG		BT136X-600E/DG,127	Tube	50	SOT186A (Halogen free)	14-Nov-2013

7. Marking

Table 4. Marking codes

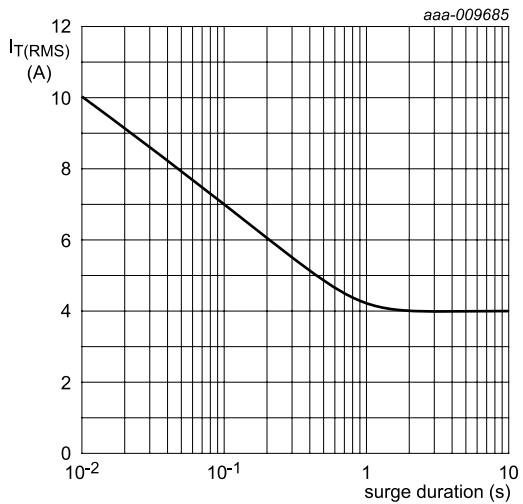
Type number	Marking codes	
	Assembly factory: d	Assembly factory: A
BT136X-600E	BT136X 600E PJdxxxx xx	BT136X 600E PJAxxxx xx
BT136X-600E/DG	BT136X 600EDG PJdxxxx xx	BT136X 600EDG PJAxxxx xx

8. Limiting values

Table 5. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions	Values	Unit
V_{DRM}	repetitive peak off-state voltage		600	V
$I_{T(RMS)}$	RMS on-state current	full sine wave; $T_h \leq 92\text{ °C}$; Fig 1 ; Fig 2 ; Fig 3	4	A
I_{TSM}	non-repetitive peak on-state current	full sine wave; $T_{j(\text{init})} = 25\text{ °C}$; $t_p = 20\text{ ms}$; Fig 4 ; Fig 5	25	A
		full sine wave; $T_{j(\text{init})} = 25\text{ °C}$; $t_p = 16.7\text{ ms}$	27	A
I^2t	I^2t for fusing	$t_p = 10\text{ ms}$; SIN	3.1	A ² s
di_T/dt	rate of rise of on-state current	$I_G = 20\text{ mA}$; T2+ G+	50	A/ μ s
		$I_G = 20\text{ mA}$; T2+ G-	50	A/ μ s
		$I_G = 20\text{ mA}$; T2- G-	50	A/ μ s
		$I_G = 50\text{ mA}$; T2- G+	10	A/ μ s
I_{GM}	peak gate current		2	A
P_{GM}	peak gate power		5	W
$P_{G(AV)}$	average gate power	over any 20 ms period	0.5	W
T_{stg}	storage temperature		-40 to 150	°C
T_j	junction temperature		125	°C



$f = 50\text{ Hz}$; $T_h = 92\text{ °C}$

Fig. 1. RMS on-state current as a function of surge duration; maximum values

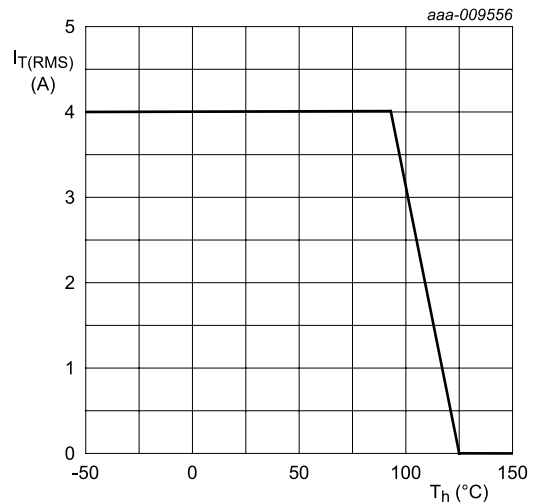


Fig. 2. RMS on-state current as a function of heatsink temperature; maximum values

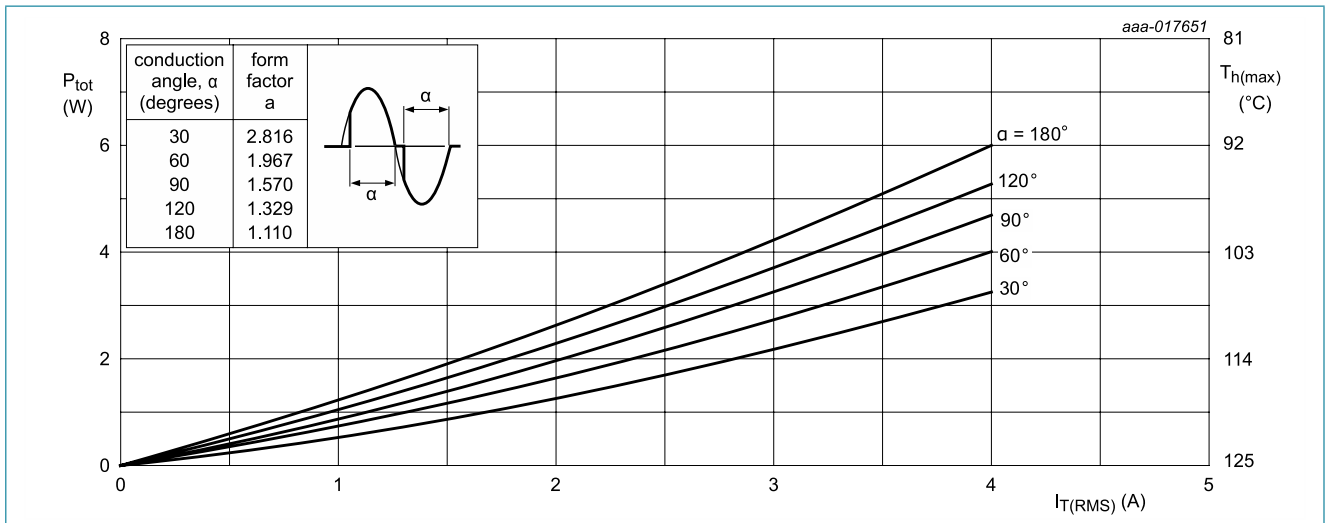


Fig. 3. Total power dissipation as a function of RMS on-state current; maximum values

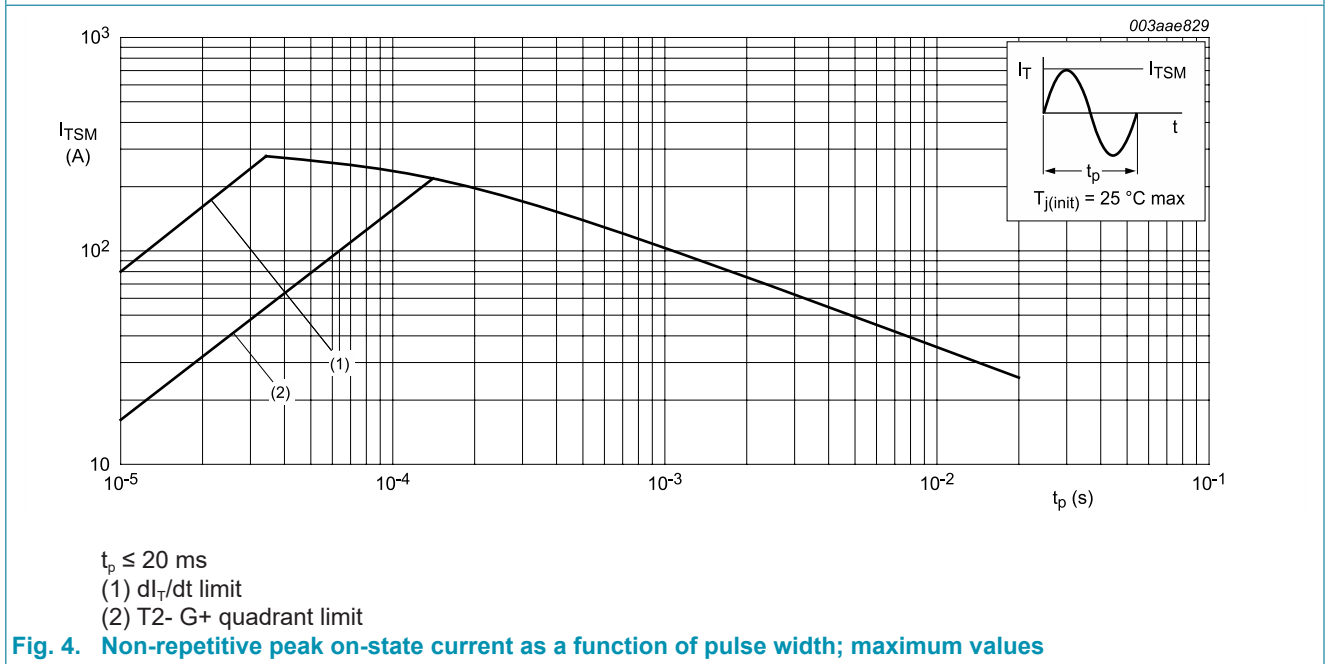
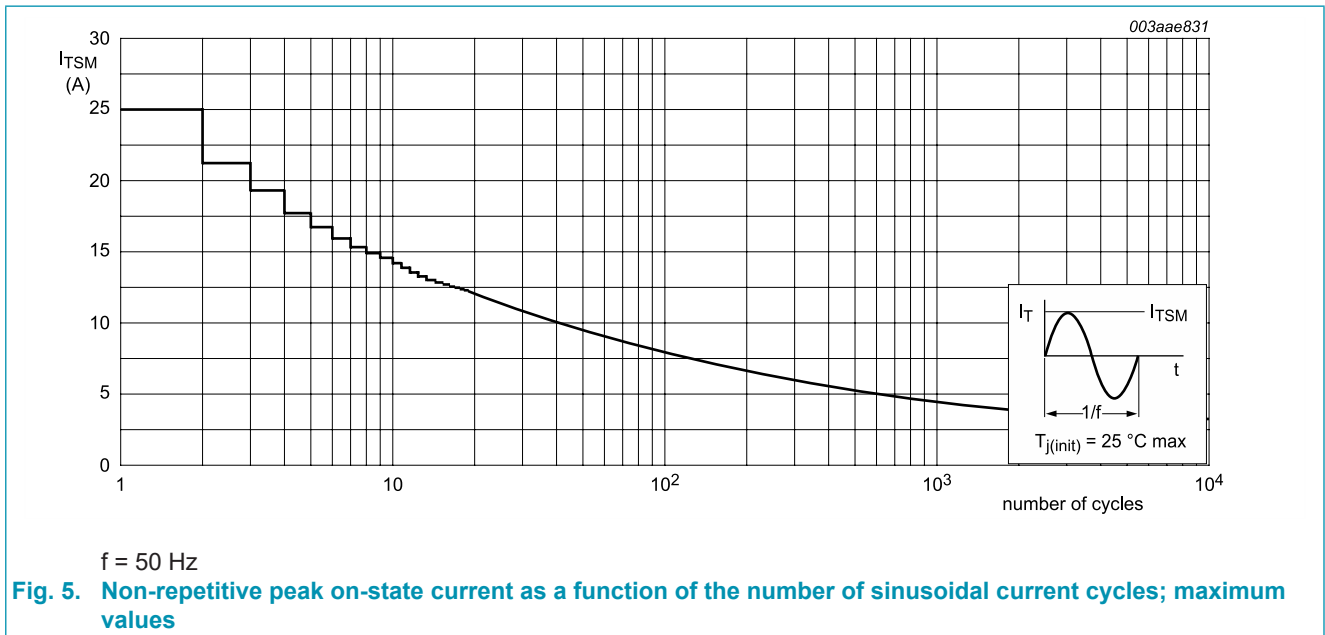


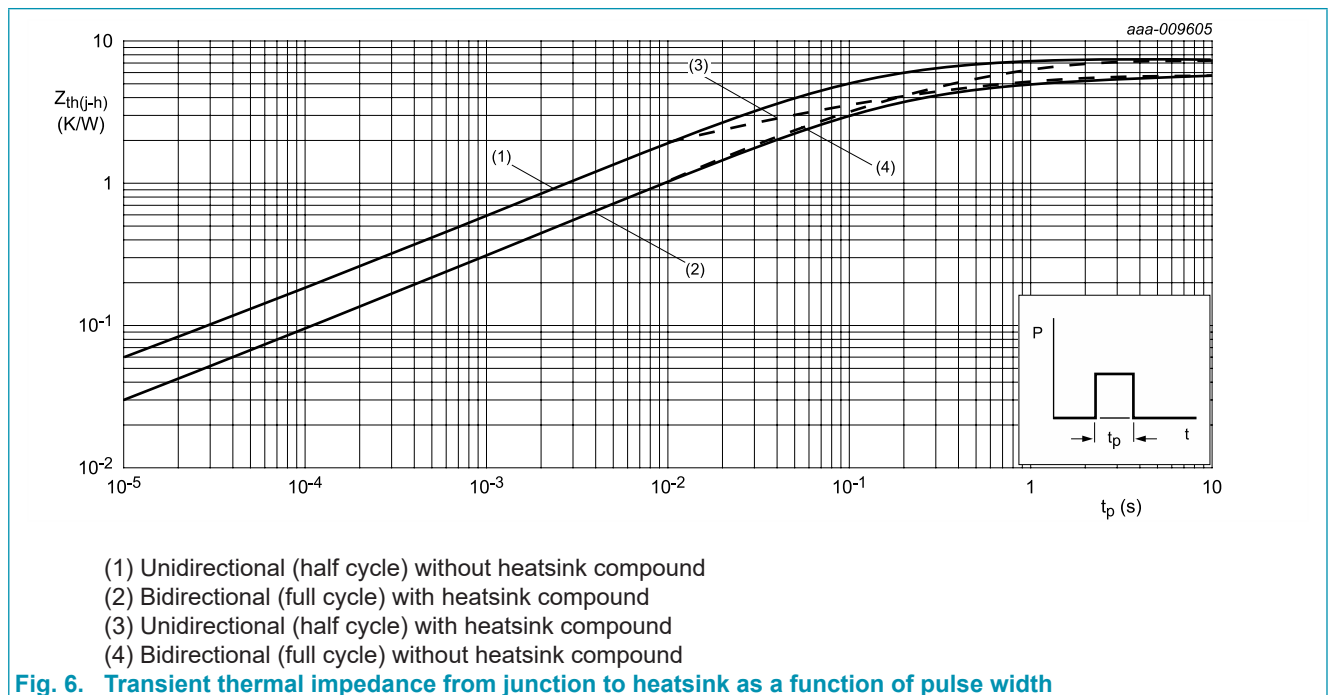
Fig. 4. Non-repetitive peak on-state current as a function of pulse width; maximum values



9. Thermal characteristics

Table 6. Thermal characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$R_{th(j-h)}$	thermal resistance from junction to heatsink	full or half cycle; with heatsink compound; Fig 6	-	-	5.5	K/W
		full or half cycle; without heatsink compound; Fig 6	-	-	7.2	K/W
$R_{th(j-a)}$	thermal resistance from junction to ambient	in free air	-	55	-	K/W



10. Isolation characteristics

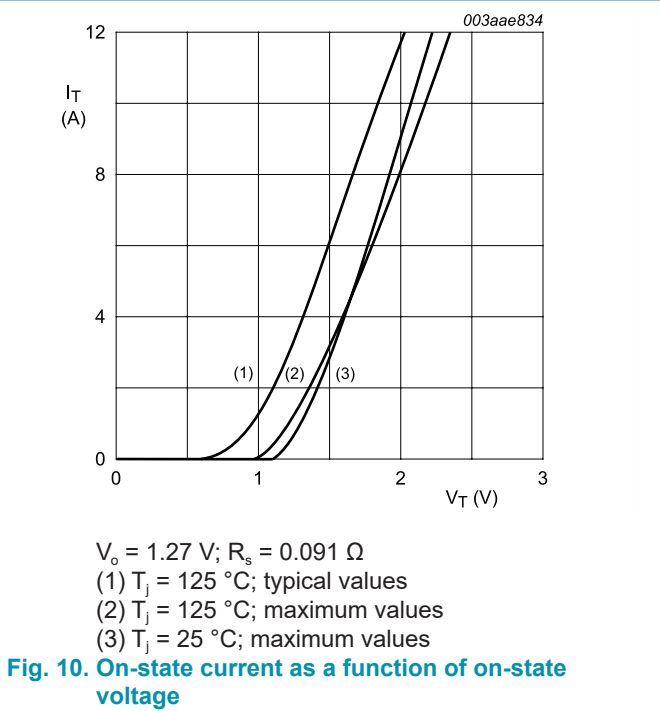
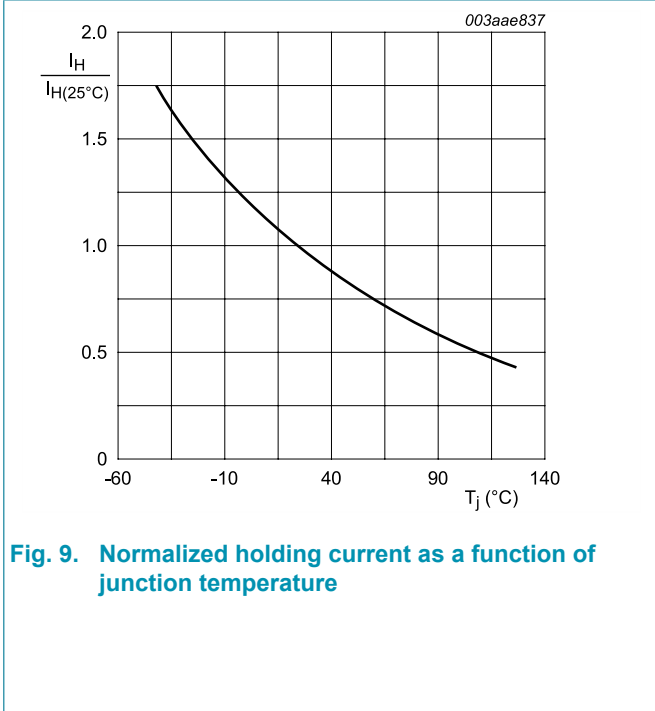
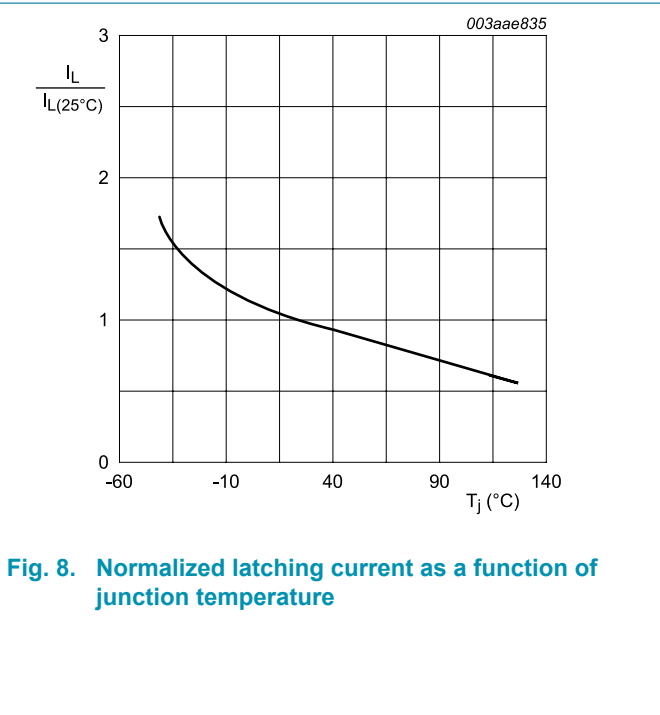
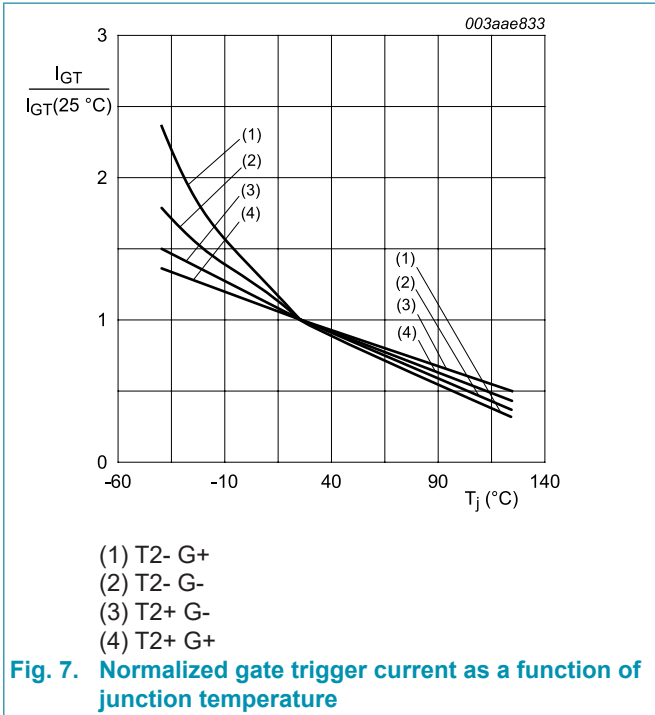
Table 7. Isolation characteristics

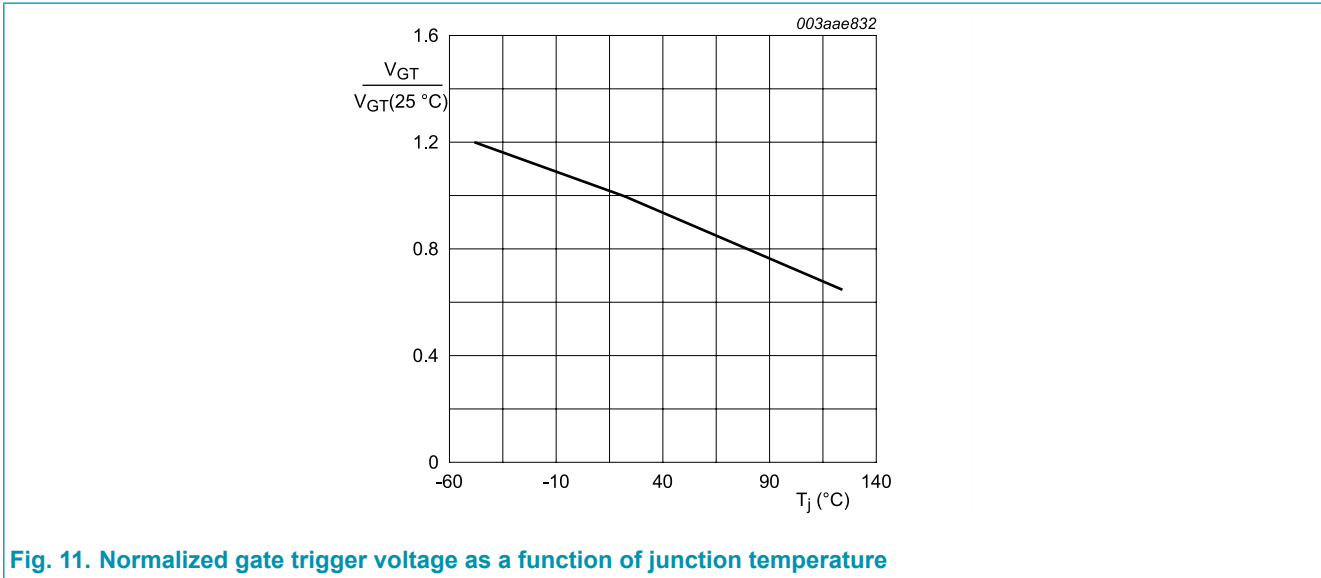
Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$V_{isol(RMS)}$	RMS isolation voltage	from all terminals to external heatsink; sinusoidal waveform; clean and dust free; 50 Hz ≤ f ≤ 60 Hz; RH ≤ 65 %; T _h = 25 °C	-	-	2500	V
C_{isol}	isolation capacitance	from main terminal 2 to external heatsink; f = 1 MHz; T _h = 25 °C	-	10	-	pF

11. Characteristics

Table 8. Characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Static characteristics						
I_{GT}	gate trigger current	$V_D = 12\text{ V}; I_T = 0.1\text{ A}; T2+ G+;$ $T_J = 25\text{ °C};$ Fig. 7	-	2.5	10	mA
		$V_D = 12\text{ V}; I_T = 0.1\text{ A}; T2+ G-;$ $T_J = 25\text{ °C};$ Fig. 7	-	4	10	mA
		$V_D = 12\text{ V}; I_T = 0.1\text{ A}; T2- G-;$ $T_J = 25\text{ °C};$ Fig. 7	-	5	10	mA
		$V_D = 12\text{ V}; I_T = 0.1\text{ A}; T2- G+;$ $T_J = 25\text{ °C};$ Fig. 7	-	11	25	mA
I_L	latching current	$V_D = 12\text{ V}; I_G = 0.1\text{ A}; T2+ G+;$ $T_J = 25\text{ °C};$ Fig. 8	-	3	15	mA
		$V_D = 12\text{ V}; I_G = 0.1\text{ A}; T2+ G-;$ $T_J = 25\text{ °C};$ Fig. 8	-	10	20	mA
		$V_D = 12\text{ V}; I_G = 0.1\text{ A}; T2- G-;$ $T_J = 25\text{ °C};$ Fig. 8	-	2.5	15	mA
		$V_D = 12\text{ V}; I_G = 0.1\text{ A}; T2- G+;$ $T_J = 25\text{ °C};$ Fig. 8	-	4	20	mA
I_H	holding current	$V_D = 12\text{ V}; T_J = 25\text{ °C};$ Fig. 9	-	2.2	15	mA
V_T	on-state voltage	$I_T = 5\text{ A}; T_J = 25\text{ °C};$ Fig. 10	-	1.4	1.7	V
V_{GT}	gate trigger voltage	$V_D = 12\text{ V}; I_T = 0.1\text{ A}; T_J = 25\text{ °C};$ Fig. 11	-	0.7	1	V
		$V_D = 400\text{ V}; I_T = 0.1\text{ A}; T_J = 125\text{ °C}$	0.25	0.4	-	V
I_D	off-state current	$V_D = 600\text{ V}; T_J = 125\text{ °C}$	-	0.1	0.5	mA
Dynamic characteristics						
dV_D/dt	rate of rise of off-state voltage	$V_{DM} = 402\text{ V}; T_J = 125\text{ °C}; (V_{DM} = 67\%$ of $V_{DRM});$ exponential waveform; gate open circuit	-	50	-	V/ μ s
t_{gt}	gate-controlled turn-on time	$V_D = 600\text{ V}; I_{TM} = 6\text{ A}; I_G = 0.1\text{ A};$ $dl_G/dt = 5\text{ A}/\mu\text{s}$	-	2	-	μ s



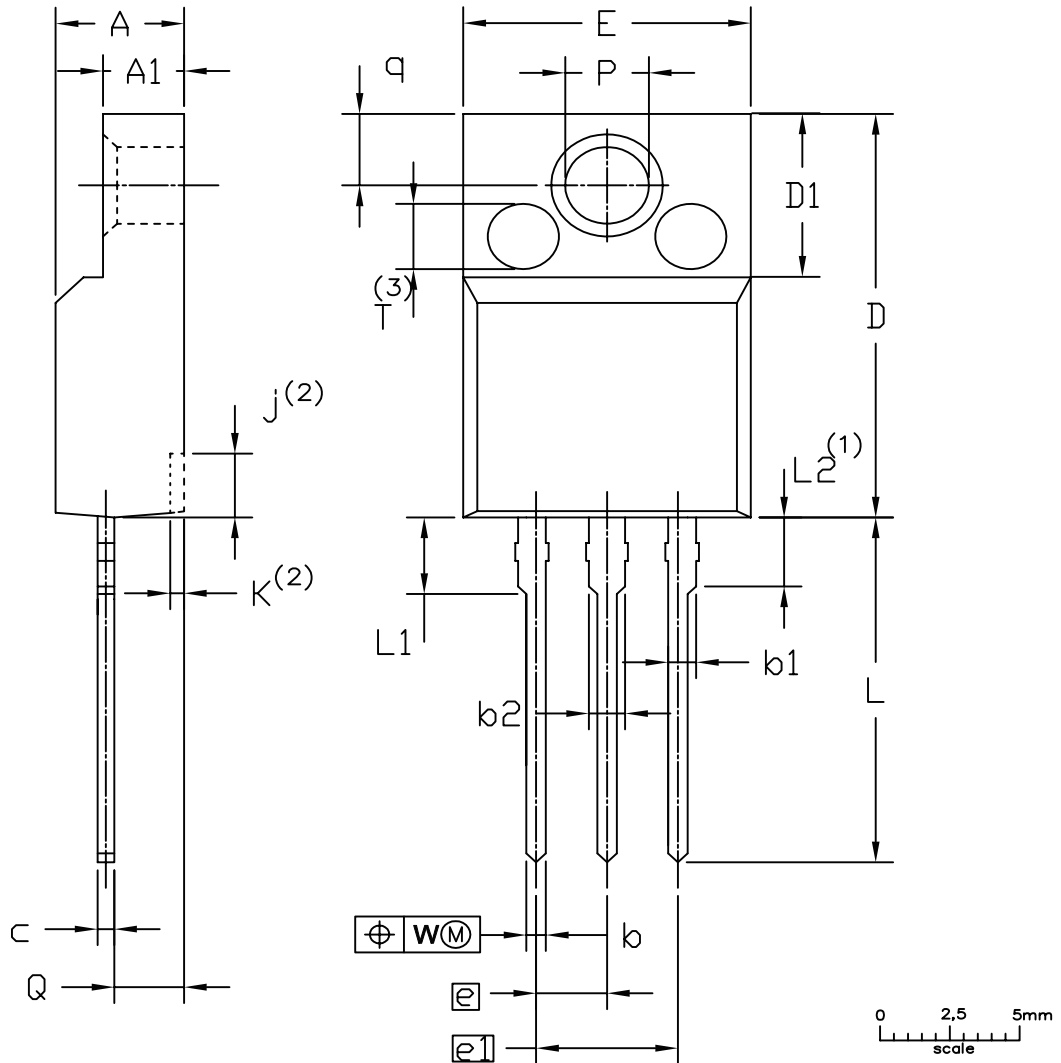


12. Package outline

Assembly factory: d & A

Plastic single-ended package; isolated heatsink mounted; 1 mounting hole; 3-lead TO-220 "full pack"

SOT186A



UNIT	A	A ₁	b	b ₁	b ₂	c	D	D ₁	E	e	e ₁	j ⁽²⁾	k ⁽²⁾	L	L ₁	L ₂ ⁽¹⁾ max.	P	Q	q	W	T ⁽³⁾
mm	4.6	2.9	0.9	1.1	1.4	0.7	15.8	6.5	10.3	2.54	5.08	2.7	0.6	14.4	3.30	3	3.2	2.6	3.0	0.4	2.5
	4.0	2.5	0.7	0.9	1.0	0.4	15.2	6.3	9.7			1.7	0.4	13.5	2.79		3.0	2.3	2.6		

Notes

1. Terminal dimensions within this zone are uncontrolled
2. Dot lines area designs may vary
3. Eject pin mark is for reference only

OUTLINE VERSION	REFERENCES			EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA		
SOT186A		3 LEADS TO220F			2013-11-14

13. Legal information

Data sheet status

Document status [1][2]	Product status [3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

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- [2] The term 'short data sheet' is explained in section "Definitions".
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